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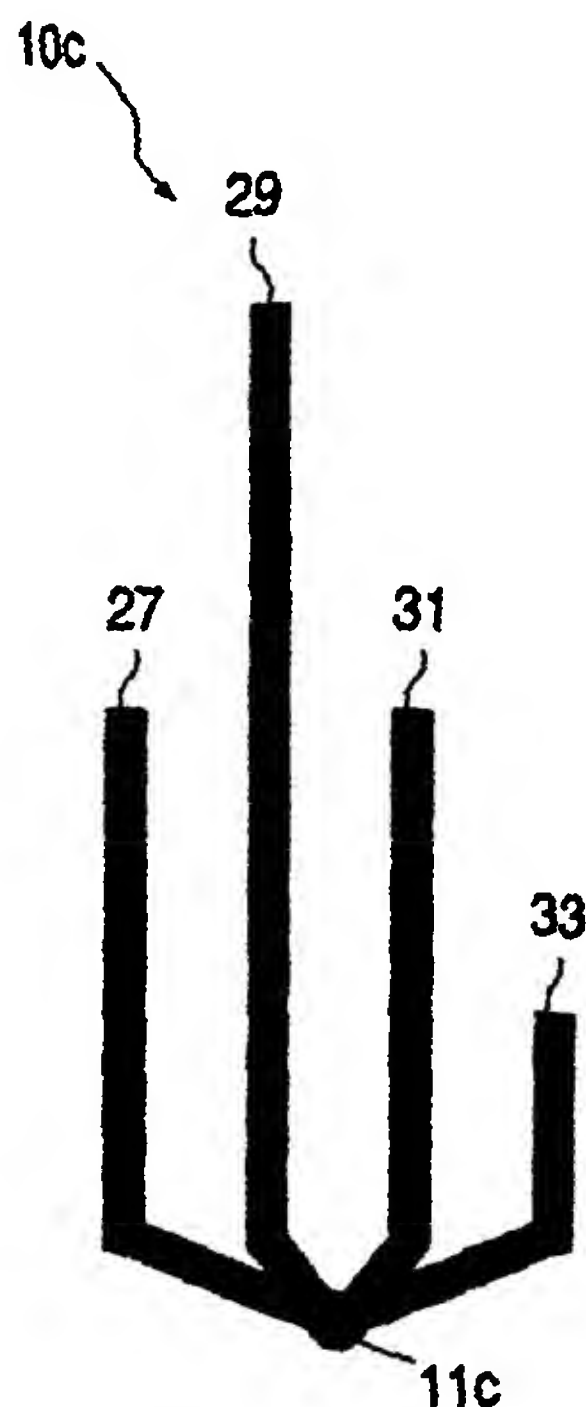
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(54) Title: VOLTAGE SUPPLY STRUCTURE AND METHOD



(57) Abstract: Fig. 1c shows a logic tree 10c comprising a plurality of logic paths (27, 29, 31, 33) connected at a root 11c. The length of each path represents the delay of the path at a nominal supply voltage. The voltage supply structure for the logic tree 10c is partitioned as shown in Fig. 3c, according to the delay of each logic path. For example, logic path (29) having the worst-case delay is supplied a voltage level V1, for example the nominal supply voltage. Logic paths (27) and (31), having a shorter delay, are supplied a second voltage level V2, which is lower than the first voltage level V1. Logic path (33), having an even shorter delay, is supplied a third voltage level V3, which is lower than V2 and V1. The voltage structure enables the voltage level and hence power consumption to be reduced without increasing the overall worst-case delay of the logic tree 10c.

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